UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,294	03/18/2004	Benjamin J. Esposito	ALTRP092/A1035	7802

51501 7590 02/20/2008

BEYER WEAVER LLP
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
YAARY, MICHAEL D	
ART UNIT	PAPER NUMBER
2193	
MAIL DATE	DELIVERY MODE
02/20/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,294	ESPOSITO ET AL.	
	Examiner	Art Unit	
	MICHAEL YAARY	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7, 11, 15, 18, 22, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magesacher et al. (hereafter Magesacher)(US Pat. 6,829,629) in view of Barnette (US Pat. 6,970,511).

4. **As to claim 1,** Magesacher discloses a multi-channel integrator (integrator of figure 1) comprising:

An integrator input (input xi of figure 1);

An integrator output (output of integrator in figure 1);

An adder (adder 12 of figure 1) comprising:

A first adder input connected to the integrator input (input xi connected to adder 12 in figure 1);

A second adder input (second input of adder 12 in figure 1); and

An adder output (output of adder 12 in figure 1);

A delay section (delay stage 14 in figure 1) comprising:

A delay section input (input to delay stage 14 in figure 1);

A delay section output (output to delay stage 14 in figure 1);

A feedback line connecting the delay section output to the second adder input (delay output feedback to adder 12 second input in figure 1);

Wherein the adder output is connected to the delay section input (adder output connected to delay stage input in delay stage 12 in figure 1); and

Further wherein the delay section output is connected to the integrator output (Integrator of figure 1 comprises multiple identical delay stages, the last delay stage 14 having an output connected to the integrator output.).

5. Magesacher does not disclose that the delay section comprises a plurality of delay elements connected in series between the delay section input and the delay section output.

However, in an analogous art, Barnette discloses a plurality of delay elements connected in series between the delay section input and the delay section output (Figure 5 and column 15, lines 64-67 disclose a delay section with multiple delay elements.).

6. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Magesacher, by implementing a plurality

of delay elements as taught by Barnette, for the benefit of being able to specifically control sampling delay time, as each delay element delays the input signal by one sample delay (Barnette, column 15, lines 64-67). One would be motivated to make the combination as to control a decimation sequence of input signals.

7. **As to claim 15.** Magesacher discloses a multi-channel differentiator (differentiator 16 in figure 2) comprising:

A differentiator input (input to differentiator circuit in figure 1);

A differentiator output (output yi to differentiator circuit in figure 1);

A subtractor (subtractor 128 in figure 2) comprising:

A first subtractor input (subtractor input to subtractor 128);

A second subtractor input (second subtractor input to subtractor 128);

A subtractor output (output of subtractor 128);

A delay section (delay section 130 in figure 1) comprising:

A delay section input connected to the differentiator input (differentiator input connected to delay element 130 input in figure 1);

A delay section output (output of delay element 130);

A feedforward line connecting the differentiator input to the first subtractor input (feedforward line to subtractor 128 in figure 1);

Wherein the delay section output is connected to the second subtractor input (delay section 130 output connected to subtractor 128 input in figure 1); and

Wherein the subtractor output is connected to the differentiator output (Differentiator of figure 1 comprises multiple identical delay stages, the last delay stage 14 having an output connected to the differentiator output).

8. Magesacher does not disclose that the delay section comprises a plurality of delay elements connected in series between the delay section input and the delay section output.

However, in an analogous art, Barnette discloses a plurality of delay elements connected in series between the delay section input and the delay section output (Figure 5 and column 15, lines 64-67 disclose a delay section with multiple delay elements.).

9. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Magesacher, by implementing a plurality of delay elements as taught by Barnette, for the benefit of being able to specifically control sampling delay time, as each delay element delays the input signal by one sample delay (Barnette, column 15, lines 64-67). One would be motivated to make the combination as to control a decimation sequence of input signals.

10. **As to claim 7 and 11,** the combination of Magesacher and Barnette disclose at least N instances of integrator of claim 1 in series (Multiple instances in the integrator and differentiator of figure 1).

11. **As to claims 18 and 22,** the combination of Magesacher and Barnette disclose at least N instances of differentiator of claim 15 in series (Multiple instances in the integrator and differentiator of figure 1).

12. **As to claim 29,** the claim is rejected for the same reasons as claim 1 above.

13. **As to claim 30,** the claim is rejected for the same reasons as claim 15 above.

14. Claims 13, 14, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magesacher and Barnette as applied to claims 1 and 15 above, and further in view of McCaslin et al. (hereafter McCaslin)(US Pat. 4,999,798).

15. McCaslin was cited in the previous office action dated 08/02/2007.

16. **As to claim 13,** the combination of Magesacher and Barnette do not disclose the integrator is implemented in a programmable device.

However, McCaslin discloses integrator is implemented in a programmable device (column 5, lines 52-57).

17. Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Magesacher, Barnette, by implementing the circuit in a programmable

device, as taught by McCaslin, in order to be able to reconfigure the device as necessary.

18. **As to claim 14,** the combination of Magesacher, Barnette, and McCaslin disclose the delay section is implemented in one or more embedded memory blocks in a programmable device (Inherent in the delay elements of McCaslin figure 2, as they need to be embedded in memory in order to operate.).

19. **As to claims 24 and 25,** the claims are rejected for the same reasons as claims 13 and 14 respectively.

20. Claims 2-6, 8-10, 12, 16, 17, 19, 20, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magesacher in view of Barnette and further in view of Applicant admitted prior art (hereafter AAPA).

21. **As to claim 2,** the combination of Magesacher and Barnette do not disclose a multi-channel numerically controlled oscillator comprising the integrator of claim 1.

However, AAPA discloses a multi-channel numerically controlled oscillator comprising the integrator of claim 1 (Page 5, lines 11-28, disclose a standard multi-channel numerically controlled oscillator).

22. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Magesacher and Barnett, by incorporating a numerically controlled oscillator with integrators and differentiators, as taught by AAPA for the benefit of generating sinusoidal signals of desired frequencies for various functions in programmable devices (AAPA page 5, lines 12-13). One would be motivated to make the combination, as an NCO is a standard known device to one of ordinary skill in the art to be used to generate a desired frequency.

23. **As to claim 3,** the combination of Magesacher, Barnette, and AAPA disclose a phase incrementer input multiplexer connected to the integrator input (AAPA, phase incrementer inputs 302a-302N in figure 3B); and

A sine/cosine generation unit connected to the integrator output (sine/cosine generator in figure 3B).

24. **As to claims 4, 5, 8, 9, and 12,** the combination of Magesacher, Barnette, and AAPA disclose the numerically controlled oscillator is an M channel numerically controlled oscillator (AAPA, inputs from 302a-302N thus having M channels) and the delay section of the integrator comprises at least M delay elements in series (Barnette, figure 5 discloses delay elements 000-004 in the delay section.).

25. **As to claim 6,** the combination of Magesacher, Barnette, and AAPA disclose a down sampler having a down-sampler input connected to the integrator output and a

down-sampler output; and a differentiator connected to the down-sampler output (AAPA, decimator of Figure 1A).

26. **As to claim 10,** the combination of Magesacher, Barnette, and AAPA disclose an up-sampler having an up-sampler output connected to the integrator input and an up-sampler input; and a differentiator connected to the up-sampler input (AAPA, interpolator of Figure 1B).

27. **As to claims 16, 19, 20 and 23,** the claims are rejected for the same reasons as claim 5, 8, 9, and 12 above as applied to the differentiator circuit of figure 1 of Magesacher.

28. **As to claim 17,** the claim is rejected for the same reasons as claim 6 above.

29. **As to claim 21,** the claim is rejected for the same reasons as claim 10 above.

30. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magesacher in view of Barnette and AAPA, and further in view of McCaslin.

31. **As to claim 26,** the claim is rejected for the same reasons as claims 1, 6, and 15 above, but the combination of Magesacher, Barnette, and AAPA do not disclose the

integration section comprising a multiplexer comprising M multiplexer inputs and a multiplexer output.

However, McCaslin discloses the integrator section comprising a multiplexer comprising M multiplexer inputs and a multiplexer output (Figure 2 and column 5, lines 15-20 disclose a multiplexer circuit 18 connected to the differentiator output. However, it would have been obvious to one of ordinary skill in the art to place a multiplexer, in similar fashion to multiplexer 18, connected to the integrator input as multiplexing many channels and signals is well known to one of ordinary skill in the art.).

32. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Magesacher, Barnette, and AAPA, by utilizing a multiplexer for the input signals, as taught by McCaslin, for the benefit of being able to selectively communicate data accordingly.

33. **As to claim 27,** the claim is rejected for the same reasons as claim 26 above and for the same reasons as recited in claim 10 above.

34. **As to claims 28,** the claim is rejected for the same reasons as claims 1-3 above.

Response to Arguments

35. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Yaary whose telephone number is (571) 270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. Y./
Examiner, Art Unit 2193

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193